

# OKI Semiconductor

## MSC23CV16458D-xxBS4

1,048,576-word x 64-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE WITH EDO

### DESCRIPTION

The MSC23CV16458D-xxBS4 is an 1,048,576-word x 64-bit CMOS dynamic random access memory module which is composed of four 16Mb(1Mx16) DRAMs in TSOP packages mounted with four decoupling capacitors. This is an 144-pin small outline dual in-line memory module. This module supports any application where high density and large capacity of storage memory are required.

### FEATURES

- 1,048,576-word x 64-bit organization
- 144-pin Small Outline Dual In-line Memory Module
- Gold tab
- Single 3.3V power supply,  $\pm 0.3V$  tolerance
- Input : LVTTTL compatible
- Output : LVTTTL compatible, 3-state
- Refresh : 1024cycles/16ms
- /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
- Fast page mode with EDO, read modify write capability

### PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation (Max.)	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating	Standby
MSC23CV16458D-50BS4	50ns	25ns	13ns	13ns	84ns	1800mW	7.2mW
MSC23CV16458D-60BS4	60ns	30ns	15ns	15ns	104ns	1656mW	
MSC23CV16458D-70BS4	70ns	35ns	20ns	20ns	124ns	1512mW	



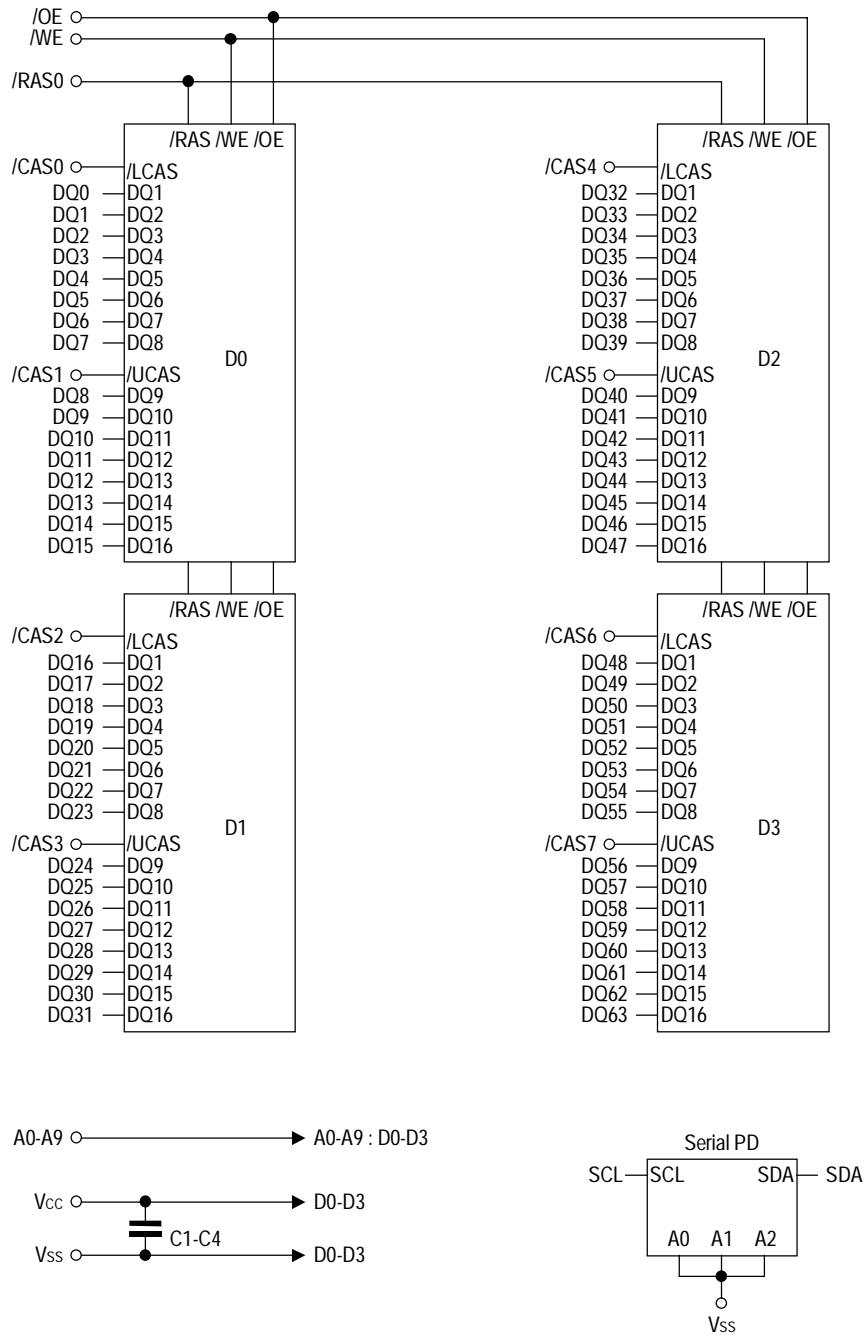
## PIN CONFIGURATION

Front Side		Back Side		Front Side		Back Side	
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>SS</sub>	2	V <sub>SS</sub>	73	/OE	74	NC
3	DQ0	4	DQ32	75	V <sub>SS</sub>	76	V <sub>SS</sub>
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V <sub>CC</sub>	82	V <sub>CC</sub>
11	V <sub>CC</sub>	12	V <sub>CC</sub>	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V <sub>SS</sub>	92	V <sub>SS</sub>
21	V <sub>SS</sub>	22	V <sub>SS</sub>	93	DQ20	94	DQ52
23	/CAS0	24	/CAS4	95	DQ21	96	DQ53
25	/CAS1	26	/CAS5	97	DQ22	98	DQ54
27	V <sub>CC</sub>	28	V <sub>CC</sub>	99	DQ23	100	DQ55
29	A0	30	A3	101	V <sub>CC</sub>	102	V <sub>CC</sub>
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	NC
35	V <sub>SS</sub>	36	V <sub>SS</sub>	107	V <sub>SS</sub>	108	V <sub>SS</sub>
37	DQ8	38	DQ40	109	A9	110	NC
39	DQ9	40	DQ41	111	NC	112	NC
41	DQ10	42	DQ42	113	V <sub>CC</sub>	114	V <sub>CC</sub>
43	DQ11	44	DQ43	115	/CAS2	116	/CAS6
45	V <sub>CC</sub>	46	V <sub>CC</sub>	117	/CAS3	118	/CAS7
47	DQ12	48	DQ44	119	V <sub>SS</sub>	120	V <sub>SS</sub>
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	V <sub>SS</sub>	56	V <sub>SS</sub>	127	DQ27	128	DQ59
57	NC	58	NC	129	V <sub>CC</sub>	130	V <sub>CC</sub>
59	NC	60	NC	131	DQ28	132	DQ60
61	NC	62	NC	133	DQ29	134	DQ61
63	V <sub>CC</sub>	64	V <sub>CC</sub>	135	DQ30	136	DQ62
65	NC	66	NC	137	DQ31	138	DQ63
67	/WE	68	NC	139	V <sub>SS</sub>	140	V <sub>SS</sub>
69	/RAS0	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	V <sub>CC</sub>	144	V <sub>CC</sub>

## Serial PD Matrix

Byte No.	Function described	SPD Value (Hex)	Note	
0	Number of Byte used	80	128 Bytes	
1	Total SPD Memory size	08	256 Bytes	
2	Memory type	02	EDO	
3	Number of Rows	0A	10	
4	Number of Columns	0A	10	
5	Number of Banks	01	1	
6	Module Data Width	40	64	
7	Module Data Width Continued	00	0	
8	Supply Voltage	01	LVTTL	
9	/RAS Access Time	-50	32	50ns
		-60	3C	60ns
		-70	46	70ns
10	/CAS Access Time	-50	0D	13ns
		-60	0F	15ns
		-70	14	20ns
11	DIMM Configuration type	00	Non-parity	
12	Refresh Rate/Type	00	Normal Refresh	
13	Primary DRAM Width	10	x16	
14	Error Checking DRAM Width	00		
15-61	Superset Information	00	Reserved	
62	SPD Data Revision Code	01	1	
63	Checksum for Byte 0-62	-50	30	
		-60	3C	
		-70	4B	
64-127	Reserved	00		
128-255	Unused Storage Location (Reserved)	FF		

BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to 4.6	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-0.5 to 4.6	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	4	W
Operating Temperature	$T_{OPR}$	0 to 70	°C
Storage Temperature	$T_{STG}$	-40 to 125	°C

\*  $T_a = 25^\circ\text{C}$

### Recommended Operating Conditions

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.0	-	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V

### Capacitance

( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	$C_{IN1}$	-	27	pF
Input Capacitance (/RAS0)	$C_{IN2}$	-	35	pF
Input Capacitance (/CAS0 - /CAS7)	$C_{IN3}$	-	13	pF
Input Capacitance (/WE)	$C_{IN4}$	-	35	pF
Input Capacitance (/OE)	$C_{IN5}$	-	35	pF
I/O Capacitance (DQ0 - DQ63)	$C_{I/O}$	-	13	pF

## DC Characteristics

 $(V_{CC} = 3.3V \pm 0.3V, T_a = 0^\circ C \text{ to } 70^\circ C)$ 

Parameter	Symbol	Condition	-50		-60		-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	$V_{OH}$	$I_{OH} = -2.0mA$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.0mA$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0V \leq V_{IN} \leq V_{CC} + 0.3V$ ; All other pins not under test = 0V	-40	40	-40	40	-40	40	$\mu A$	
Output Leakage Current	$I_{LO}$	DQ disable $0V \leq V_{OUT} \leq V_{CC}$	-10	10	-10	10	-10	10	$\mu A$	
Average Power Supply Current (Operating)	$I_{CC1}$	/RAS, /CAS cycling, $t_{RC} = \text{Min.}$	-	500	-	460	-	420	mA	1, 2
Power Supply Current (Standby)	$I_{CC2}$	/RAS, /CAS = $V_{IH}$	-	8	-	8	-	8	mA	1
		/RAS, /CAS $\geq V_{CC} - 0.2V$	-	2	-	2	-	2	mA	
Average Power Supply Current (/RAS only refresh)	$I_{CC3}$	/RAS cycling, /CAS = $V_{IH}$ , $t_{RC} = \text{Min.}$	-	500	-	460	-	420	mA	1, 2
Average Power Supply Current (/CAS before /RAS refresh)	$I_{CC6}$	/RAS cycling, /CAS before /RAS	-	500	-	460	-	420	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	/RAS = $V_{IL}$ , /CAS cycling, $t_{HPC} = \text{Min.}$	-	500	-	460	-	420	mA	1, 3

- Notes: 1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.  
2. The address can be changed once or less while /RAS =  $V_{IL}$ .  
3. The address can be changed once or less while /CAS =  $V_{IH}$ .

## AC Characteristics (1/2)

(V<sub>CC</sub> = 3.3V ±0.3V, Ta = 0°C to 70°C) Note: 1, 2, 3

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	84	-	104	-	124	-	ns	
Read Modify Write Cycle Time	t <sub>RWC</sub>	110	-	135	-	160	-	ns	
Fast Page Mode Cycle Time	t <sub>HPC</sub>	20	-	25	-	30	-	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>HRWC</sub>	58	-	68	-	78	-	ns	
Access Time from /RAS	t <sub>RAC</sub>	-	50	-	60	-	70	ns	4, 5, 6
Access Time from /CAS	t <sub>CAC</sub>	-	13	-	15	-	20	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	-	25	-	30	-	35	ns	4, 6
Access Time from /CAS Precharge	t <sub>CPA</sub>	-	30	-	35	-	40	ns	4
Access Time from /OE	t <sub>OEA</sub>	-	13	-	15	-	20	ns	4
Output Low Impedance Time from /CAS	t <sub>CLZ</sub>	0	-	0	-	0	-	ns	4
Data Output Hold After /CAS Low	t <sub>DOH</sub>	5	-	5	-	5	-	ns	
/CAS to Data Output Buffer Turn-off Delay Time	t <sub>CEZ</sub>	0	13	0	15	0	20	ns	7, 8
/RAS to Data Output Buffer Turn-off Delay Time	t <sub>REZ</sub>	0	13	0	15	0	20	ns	7, 8
/OE to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	0	13	0	15	0	20	ns	7
/WE to Data Output Buffer Turn-off Delay Time	t <sub>WEZ</sub>	0	13	0	15	0	20	ns	7
Transition Time	t <sub>T</sub>	1	50	1	50	1	50	ns	3
Refresh Period	t <sub>REF</sub>	-	16	-	16	-	16	ms	
/RAS Precharge Time	t <sub>RP</sub>	30	-	40	-	50	-	ns	
/RAS Pulse Width	t <sub>RAS</sub>	50	10K	60	10K	70	10K	ns	
/RAS Pulse Width (Fast Page Mode with EDO)	t <sub>RASP</sub>	50	100K	60	100K	70	100K	ns	
/RAS Hold Time	t <sub>RSH</sub>	7	-	10	-	13	-	ns	
/RAS Hold Time referenced to /OE	t <sub>ROH</sub>	7	-	10	-	13	-	ns	
/CAS Precharge Time (Fast Page Mode with EDO)	t <sub>CP</sub>	7	-	10	-	10	-	ns	
/CAS Pulse Width	t <sub>CAS</sub>	7	10K	10	10K	13	10K	ns	
/CAS Hold Time	t <sub>CSH</sub>	35	-	40	-	45	-	ns	
/CAS to /RAS Precharge Time	t <sub>CRP</sub>	5	-	5	-	5	-	ns	
/RAS Hold Time from /CAS Precharge	t <sub>RHCP</sub>	30	-	35	-	40	-	ns	
/OE Hold Time from /CAS (DQ Disable)	t <sub>CHO</sub>	5	-	5	-	5	-	ns	
/RAS to /CAS Delay Time	t <sub>RCD</sub>	11	37	14	45	14	50	ns	5
/RAS to Column Address Delay Time	t <sub>RAD</sub>	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	-	0	-	0	-	ns	
Row Address Hold Time	t <sub>RAH</sub>	7	-	10	-	10	-	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	-	0	-	0	-	ns	
Column Address Hold Time	t <sub>CAH</sub>	7	-	10	-	13	-	ns	
Column Address to /RAS Lead Time	t <sub>RAL</sub>	25	-	30	-	35	-	ns	



**AC Characteristics (2/2)**

( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_a = 0^{\circ}C$  to  $70^{\circ}C$ ) Note: 1, 2, 3

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	$t_{RCS}$	0	-	0	-	0	-	ns	
Read Command Hold Time	$t_{RCH}$	0	-	0	-	0	-	ns	9
Read Command Hold Time referenced to /RAS	$t_{RRH}$	0	-	0	-	0	-	ns	9
Write Command Set-up Time	$t_{WCS}$	0	-	0	-	0	-	ns	10
Write Command Hold Time	$t_{WCH}$	7	-	10	-	13	-	ns	
Write Command Pulse Width	$t_{WP}$	7	-	10	-	10	-	ns	
/WE Pulse Width (DQ Disable)	$t_{WPE}$	7	-	10	-	10	-	ns	
/OE Command Hold Time	$t_{OEH}$	7	-	10	-	13	-	ns	
/OE Precharge Time	$t_{OEP}$	7	-	10	-	10	-	ns	
/OE Command Hold Time	$t_{OCH}$	7	-	10	-	10	-	ns	
Write Command to /RAS Lead Time	$t_{RWL}$	7	-	10	-	13	-	ns	
Write Command to /CAS Lead Time	$t_{CWL}$	7	-	10	-	13	-	ns	
Data-in Set-up Time	$t_{DS}$	0	-	0	-	0	-	ns	
Data-in Hold Time	$t_{DH}$	7	-	10	-	13	-	ns	
/OE to Data-in Delay Time	$t_{OED}$	13	-	15	-	20	-	ns	
/CAS to /WE Delay Time	$t_{CWD}$	30	-	34	-	44	-	ns	10
Column Address to /WE Delay Time	$t_{AWD}$	42	-	49	-	59	-	ns	10
/RAS to /WE Delay Time	$t_{RWD}$	67	-	79	-	94	-	ns	10
/CAS Precharge /WE Delay Time	$t_{CPWD}$	47	-	54	-	64	-	ns	10
/CAS Active Delay Time from /RAS Precharge	$t_{RPC}$	5	-	5	-	5	-	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	$t_{CSR}$	5	-	5	-	5	-	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	$t_{CHR}$	10	-	10	-	10	-	ns	

- Notes:
1. A start-up delay of 200 $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 2$ ns.
  3.  $V_{IH}(\text{Min.})$  and  $V_{IL}(\text{Max.})$  are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100pF. The output timing reference levels are  $V_{OH} = 2.0$ V and  $V_{OL} = 0.8$ V.
  5. Operation within the  $t_{RCD}(\text{Max.})$  limit ensures that  $t_{RAC}(\text{Max.})$  can be met.  $t_{RCD}(\text{Max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{Max.})$  limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}(\text{Max.})$  limit ensures that  $t_{RAC}(\text{Max.})$  can be met.  $t_{RAD}(\text{Max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{Max.})$  limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{CEZ}(\text{Max.})$ ,  $t_{REZ}(\text{Max.})$ ,  $t_{WEZ}(\text{Max.})$  and  $t_{OEZ}(\text{Max.})$  define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{CEZ}$  or  $t_{REZ}$  must be satisfied for open circuit condition.
  9.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  10.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{Min.})$ , then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{Min.})$ ,  $t_{RWD} \geq t_{RWD}(\text{Min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{Min.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{Min.})$ , then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.